AMENDMENT

In The Claim

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1. (Once Amended) A memory device, comprising

a substrate;

a gate oxide layer, disposed on a surface of the substrate;

a gate, disposed on a portion of the gate oxide layer;

a buried drain line, located in the substrate beside both sides of the gate;

a spacer, disposed on sidewalls of the gate;

a deep doped region, located in the substrate below a part of the buried drain line, wherein the buried drain line and the deep doped region together form a bit line of the memory device;

an insulation layer, disposed on the gate oxide layer and above the bit line; and

a word line, disposed above the gate and the insulation layer, perpendicular to a direction of the bit line.

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6. (Once Amended) A fabrication method for a memory device, comprising:

forming a gate oxide layer on a substrate;

forming a bar-shaped conductive structure on the gate oxide layer, wherein a cap layer is formed on a top of the bar-shaped conductive structure;

forming a buried drain line in the substrate beside both sides of the bar-shaped conductive structure;

forming a spacer on sidewalls of the bar-shaped conductive structure and the cap layer;

forming a deep doped region in the substrate beside both sides of the spacer, wherein the